

Claims

What is claimed is:

1. A processor comprising:

controller circuitry configurable to determine for a given protocol data unit received

5 by the processor whether the given protocol data unit is a single-cell protocol data unit; and

first memory circuitry internal to the processor;

the processor being connectable to second memory circuitry external to the processor;

wherein information characterizing the given protocol data unit is stored in the first
memory circuitry if the given protocol data unit is a single-cell protocol data unit; and

10 wherein information characterizing the given protocol data unit is stored in the second
memory circuitry if the given protocol data unit is not a single-cell protocol data unit.

2. The processor of claim 1 wherein the protocol data unit comprises a packet.

15 3. The processor of claim 1 wherein the single-cell protocol data unit comprises a protocol
data unit having a size less than or substantially equal to that of a cell-based processing unit of a
switch fabric associated with the processor.

20 4. The processor of claim 1 wherein the information characterizing the given protocol data
unit comprises at least one block descriptor.

5. The processor of claim 4 wherein the block descriptor is associated with a particular data
block of the given protocol data unit.

25 6. The processor of claim 1 wherein the information characterizing the given protocol data
unit is stored in the first memory circuitry without requiring utilization of a linked list data structure.

7. The processor of claim 1 wherein the information characterizing the given protocol data unit is stored in the second memory circuitry utilizing a linked list data structure.

5 8. The processor of claim 1 wherein the processor is configured to provide an interface for communication of the protocol data unit between a network and a switch fabric.

9. The processor of claim 1 wherein at least one of the first memory circuitry and the second memory circuitry further comprises a queuing and dispatch buffer memory of the processor.

10 10. The processor of claim 1 wherein at least one of the first memory circuitry and the second memory circuitry further comprises a PDU buffer memory of the processor.

11. The processor of claim 1 wherein the processor comprises a network processor.

15 12. The processor of claim 1 wherein the processor is configured as an integrated circuit.

13. A method for use in a processor comprising controller circuitry and first memory circuitry internal to the processor, the processor being connectable to second memory circuitry external to the processor, the method comprising the steps of:

20 determining for a given protocol data unit received by the processor whether the given protocol data unit is a single-cell protocol data unit;

storing information characterizing the given protocol data unit in the first memory circuitry if the given protocol data unit is a single-cell protocol data unit; and

25 storing information characterizing the given protocol data unit in the second memory circuitry if the given protocol data unit is not a single-cell protocol data unit.

14. An article of manufacture comprising a machine-readable storage medium having program code stored thereon for use in a processor comprising controller circuitry and first memory

circuitry internal to the processor, the processor being connectable to second memory circuitry external to the processor, the program code when executed in the processor implementing the steps of:

- 5 determining for a given protocol data unit received by the processor whether the given protocol data unit is a single-cell protocol data unit;
 - storing information characterizing the given protocol data unit in the first memory circuitry if the given protocol data unit is a single-cell protocol data unit; and
 - storing information characterizing the given protocol data unit in the second memory circuitry if the given protocol data unit is not a single-cell protocol data unit.

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